Version with Markings to Show Changes Made

IN THE SPECIFICATION:

PAGE 3, PARAGRAPH 2 (a.k.a. lines 9-21) has been amended as follows:

An embodiment of the invention uses standard clock signals, a delay element that can be as simple as a series of inverters, and an enabled latch to interface static logic to dynamic logic. The inverse of the dynamic logic evaluate clock is fed to the clock input of a transparent latch with clock and enable inputs. A delayed version of this clock is generated by the delay element. This delayed inverse of the dynamic logic evaluate clock is fed to the enable input of the latch. The input to the latch comes from static logic and the output of the latch is fed to the dynamic logic. The net result is a latch that is open until the evaluate clock is instructing the dynamic logic to ~~reset, or precharge,~~ evaluate and remains closed until a delay element delay time after the evaluate clock instructs the dynamic logic to reset.

PAGE 4, PARAGRAPH 1 (a.k.a. lines 2-10) has been amended as follows:

FIG. 1 is a schematic illustration of a static to dynamic logic interface that produces a monotonic output. In FIG. 1, IN is the input signal from static logic. OUT is the output signal that may be connected to dynamic logic. CK is the inverse of the dynamic logic evaluate clock. In the embodiment shown in FIG. 1, when CK is ~~high~~ low it is the dynamic logic evaluate phase. CK is input to delay element **104**. The output of delay element is a delayed version of CK called CKD. Delay element **104** may be as simple as an even number of inverters. CK is also connected to the clock input of a transparent latch **102** and CKD is connected to an enable input of transparent latch **102**.